AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A memory integrated circuit comprising:

one or more data input/output terminals;

an input buffer; and

a state decoder for receiving a chip select signal targeted for the memory integrated circuit; and

a parasitic capacitance control bus switch having an input portion connected to said one or more data input/output terminals, and an output portion connected to said input buffer, wherein the switch is an integral part of the memory integrated circuit, and wherein the input buffer is selectively decoupled from the terminals in response to a change in state in the chip select signal, ~~and wherein~~ the switch ~~is~~ being operated so as to control the parasitic capacitance of the terminals in response to receiving the chip select signal.

2. (Currently Amended) A memory integrated circuit comprising:

a contact which connects to a data bus; and

a parasitic capacitance control switch, wherein an input portion of said switch is connected to said contact, ~~wherein~~ the switch ~~is~~ being operated so as to control the parasitic capacitance of the terminals.

3. (Previously Presented) The integrated circuit of Claim 2 wherein an output portion of said switch is connected to one or more buffers.

4. (Currently Amended) A memory integrated circuit comprising:

one or more data input/output terminals;

an input buffer; and

a parasitic capacitance control bus switch having an input portion connected to said one or more data input/output terminals, and an output portion connected to said input buffer, ~~wherein~~ the switch ~~is~~ being operated so as to control the parasitic capacitance of the input/output terminals; and

one or more control terminals for receiving memory access control signals, and wherein ~~said~~ a logic circuit is coupled to at least one of said one or more control terminals.

5. (Original) The memory integrated circuit of Claim 4, wherein said bus switch further comprises a control portion coupled to a logic circuit on said memory integrated circuit, where in said logic circuit is configured to selectively open said bus switch during at least a portion of a memory access cycle.

6. (Original) The memory integrated circuit of Claim 4, wherein said memory integrated circuit further comprises one or more control terminals for receiving memory access control signals, and wherein said logic circuit is coupled to at least one of said one or more control terminals.

7. (Currently Amended) A memory integrated circuit comprising:

one or more data input/output terminals;

an input buffer; and

a parasitic capacitance control bus switch having an input portion connected to said one or more data input/output terminals, and an output portion connected to said input buffer, wherein the switch is an integral part of the memory integrated circuit, ~~wherein~~ the switch ~~is~~ being operated so as to control the parasitic capacitance of the input/output terminals; and

one or more control terminals for receiving memory access control signals, and wherein a logic circuit is coupled to at least one of said one or more control terminals.

8. (Currently Amended) A memory integrated circuit comprising:

one or more data input/output terminals;

an input buffer;

a state decoder for receiving chip select signal targeted for the input buffer ~~memory circuit~~;

a parasitic capacitance control bus switch having an input portion connected to said one or more data input/output terminals, and an output portion connected to said input buffer, wherein the input buffer is selectively decoupled from the bus in response to a change in state in the chip select signal, ~~wherein~~ the switch ~~is~~ being operated so as to control the parasitic capacitance of the input/output terminals in response to the chip select signal; and

one or more control terminals for receiving memory access control signals, and wherein a logic circuit is coupled to at least one of said one or more control terminals.

9. (Currently Amended) A method of transferring data, the method comprising:

disabling a transfer gate when no memory access are occurring;

enabling a transfer gate when memory accesses are occurring, ~~wherein~~ the transfer gate ~~is~~ being operated so as to control the parasitic capacitance of a bus;

wherein enabling and disabling occur in a memory integrated circuit.

10. (Previously Presented) The method of Claim 9, wherein the memory integrated circuit additionally comprises a contact which connects to a data bus and a switch, wherein an input portion of said switch is connected to the contact, wherein an output portion of said switch is connected to one or more buffer buffers , the method further comprising, transferring data to and from the buffers subsequent to enabling the transfer gate.

11. (Currently Amended) A system for transferring data, the system comprising:

means for disabling a transfer gate when no memory access are occurring;

means for enabling a transfer gate when memory accesses are occurring, ~~wherein~~ the means for enabling and the means for disabling being ~~switch is~~ operated so as to control the parasitic capacitance of a bus; and

wherein the means for enabling and the means for disabling reside within a memory integrated circuit.